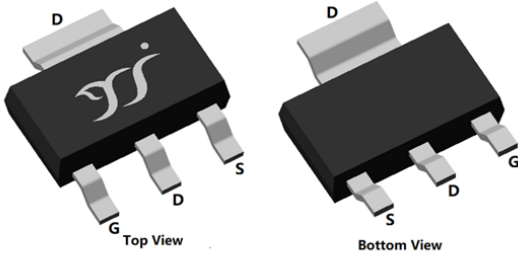
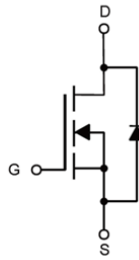


N-Channel Enhancement Mode Field Effect Transistor



SOT-223



Product Summary

- V_{DS} 650V
- I_D 0.5A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<2.5\Omega$

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings ($T_J=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-source Voltage		V_{DS}	650	V	
Gate-source Voltage		V_{GS}	± 30	V	
Continuous Drain Current (Note 1,2)	Steady-State	I_D	$T_A=25^\circ C, V_{GS}=10V$	0.5	A
			$T_A=100^\circ C, V_{GS}=10V$	0.3	
Pulsed Drain Current	$T_C=25^\circ C, t_p=100\mu s$		I_{DM}	3	A
Total Power Dissipation (Note 1,2)	Steady-State	P_D	$T_A=25^\circ C$	1.56	W
			$T_A=100^\circ C$	0.62	
MOSFET dv/dt ruggedness	$V_{DS}=0\dots 325V, R_g=0\Omega$		dv/dt	8.4	V/ns
Reverse diode dv/dt	$V_{DS}=0\dots 325V, I_D \le 0.5A, di/dt=100A/\mu s$		dv/dt	13.7	
Insulation withstand voltage	$V_{rms}, t=5s$		V_{ISO}	1000	V
Junction and Storage Temperature Range			T_J, T_{STG}	-55~+150	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	65	80	$^\circ C/W$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJM2K5C65BHJ	F2	2K5C65	2500	5000	25000	13" reel



YJM2K5C65BHJ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V	-	-	10	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.7	3.5	4.3	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =0.5A	-	2.1	2.5	Ω
Diode Forward Voltage	V _{SD}	I _S =0.5A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	8.5	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	0.5	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =325V, V _{GS} =0V, f=1MHz	-	89	-	pF
Output Capacitance	C _{oss}		-	4	-	
Reverse Transfer Capacitance	C _{rss}		-	0.9	-	
Effective output capacitance, energy related	C _{o(er)}	V _{DS} =0...325V, V _{GS} =0V, f=1MHz	-	6.6	-	pF
Effective output capacitance, time related	C _{o(tr)}		-	33	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =325V, I _D =0.5A	-	3.9	-	nC
Gate-Source Charge	Q _{gs}		-	0.57	-	
Gate-Drain Charge	Q _{gd}		-	2.37	-	
Reverse Recovery Charge	Q _{rr}	I _F =0.5A, di/dt=100A/us	-	225.5	-	nC
Reverse Recovery Time	t _{rr}		-	91.2	-	ns
Peak reverse recovery current	I _{rrm}		-	4.65	-	A
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =325V, I _D =0.5A R _{GEN} =3Ω	-	19.2	-	ns
Turn-on Rise Time	t _r		-	23.7	-	
Turn-off Delay Time	t _{D(off)}		-	21.6	-	
Turn-off fall Time	t _f		-	43.3	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



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Typical Electrical and Thermal Characteristics Diagrams

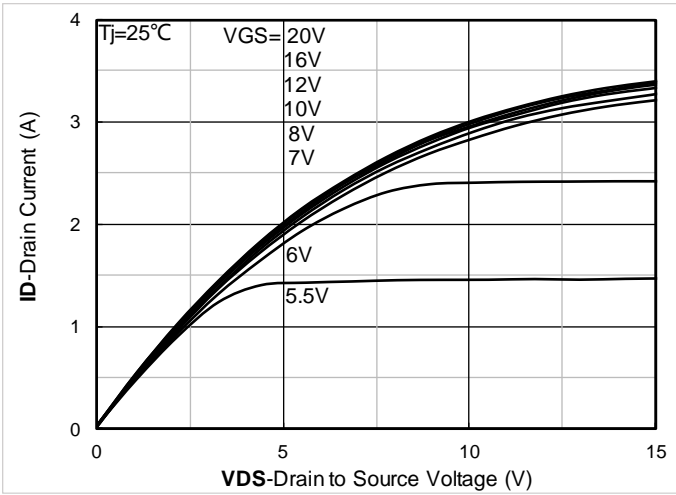


Figure 1. Output Characteristics

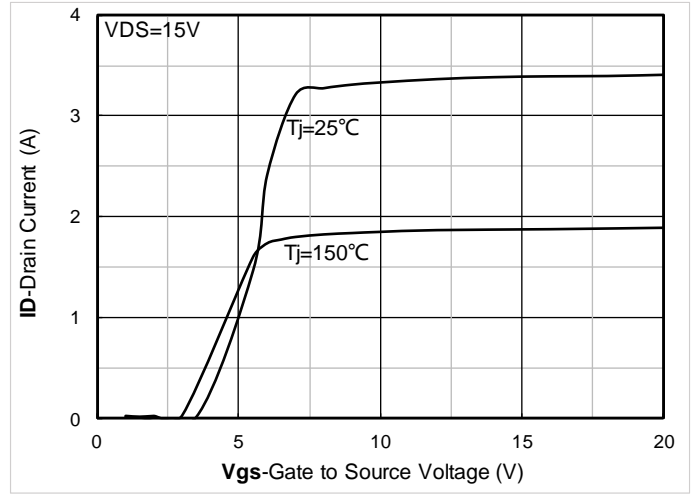


Figure 2. Transfer Characteristics

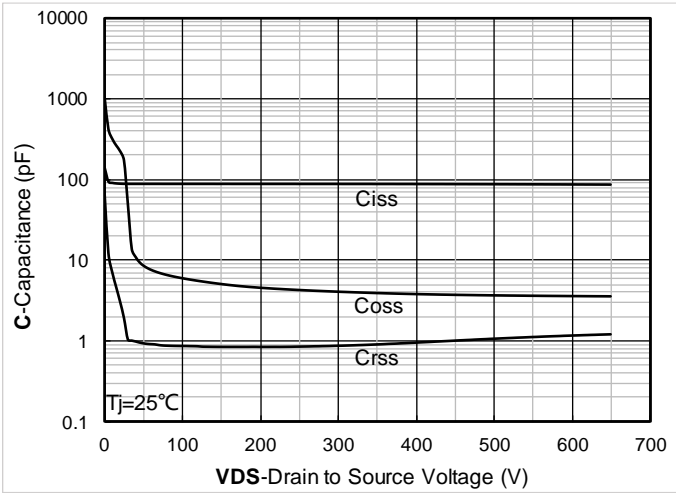


Figure 3. Capacitance Characteristics

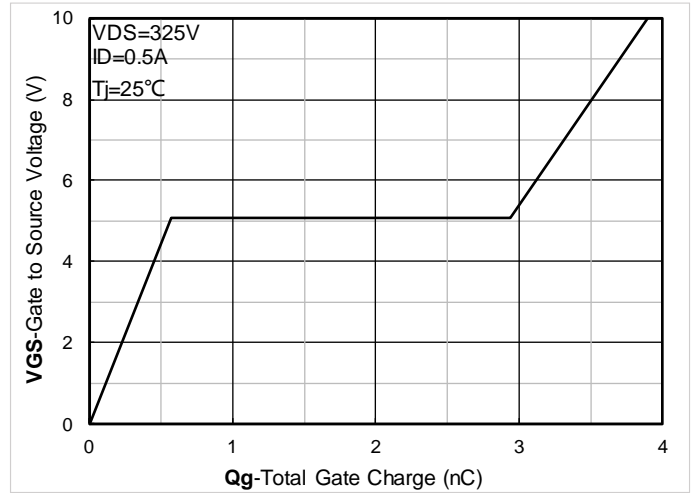


Figure 4. Gate Charge

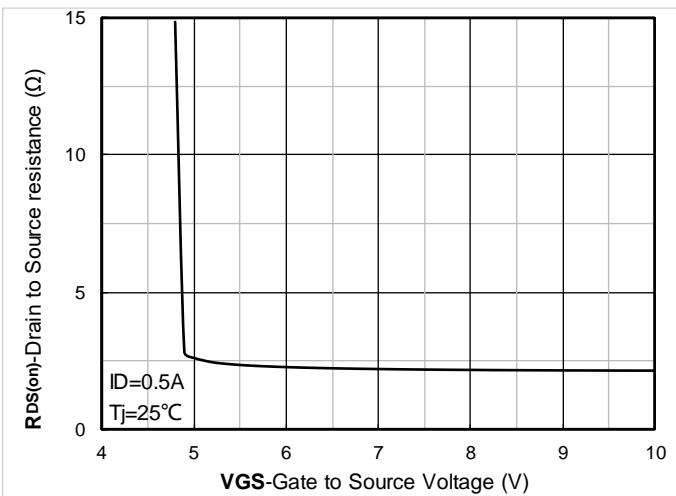


Figure 5. On-Resistance vs Gate to Source Voltage

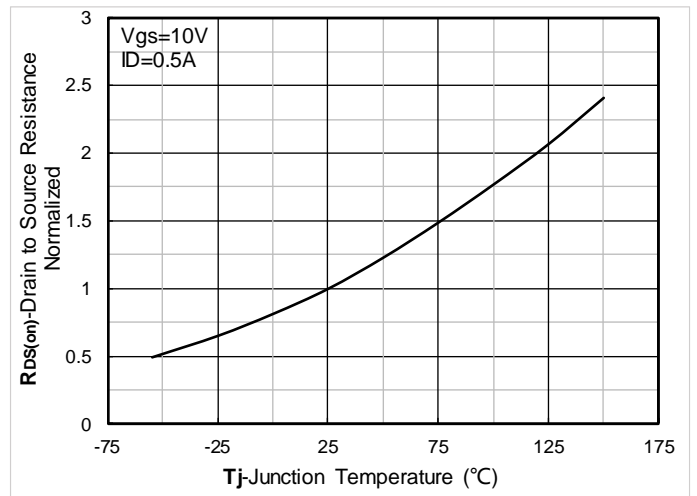


Figure 6. Normalized On-Resistance



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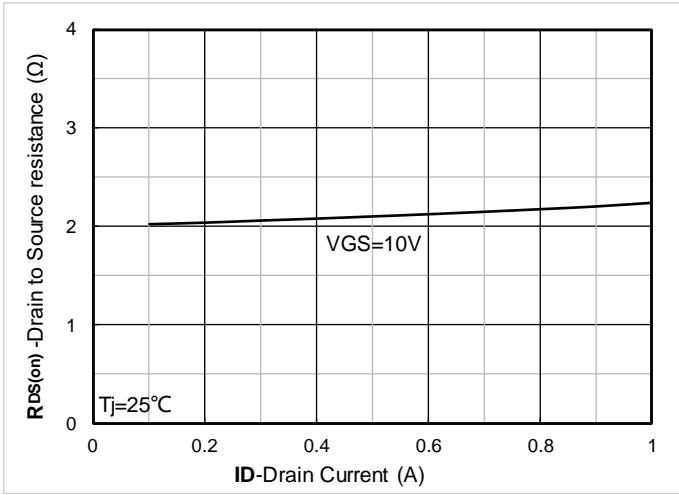


Figure 7. $R_{DS(on)}$ VS Drain Current

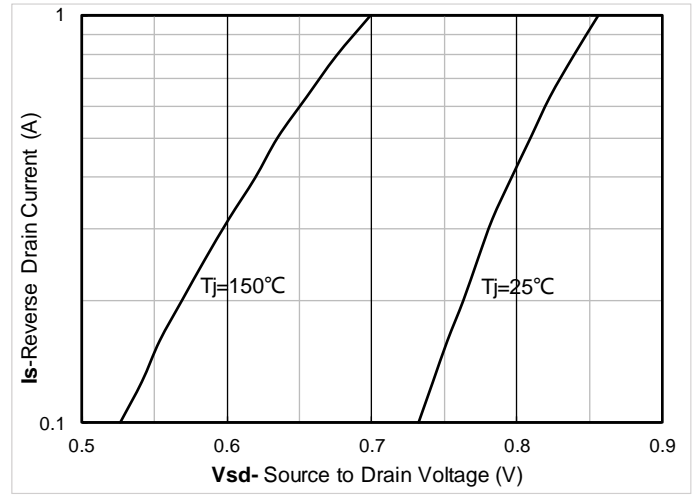


Figure 8. Forward characteristics of reverse diode

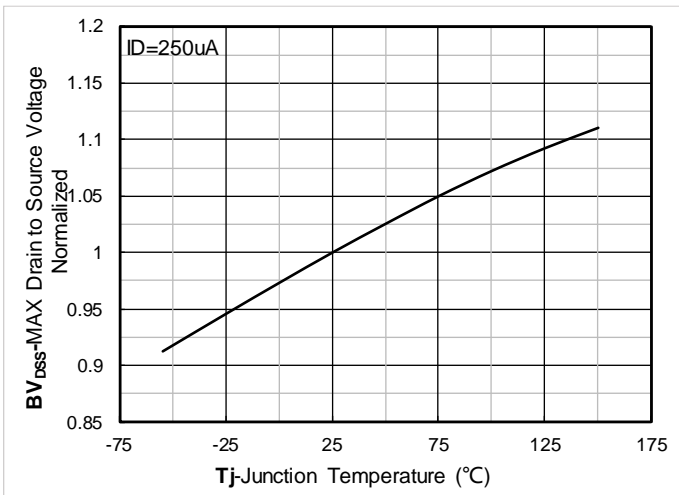


Figure 9. Normalized breakdown voltage

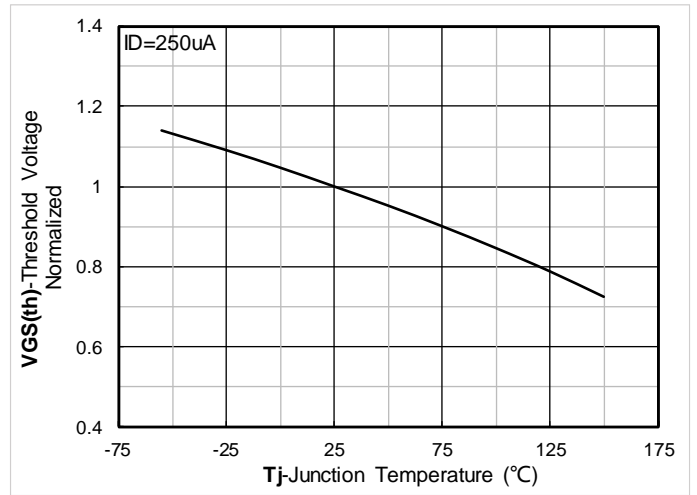


Figure 10. Normalized Threshold voltage

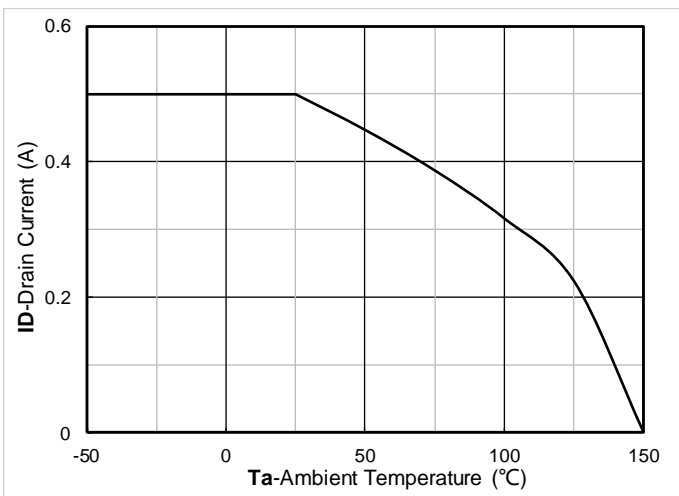


Figure 11. Current dissipation

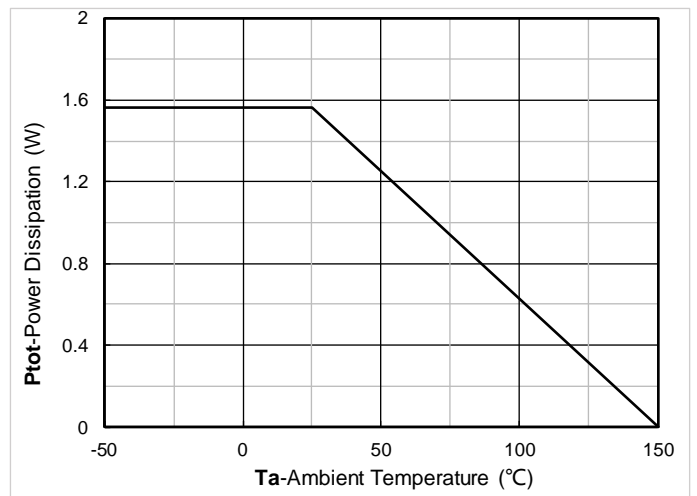


Figure 12. Power dissipation

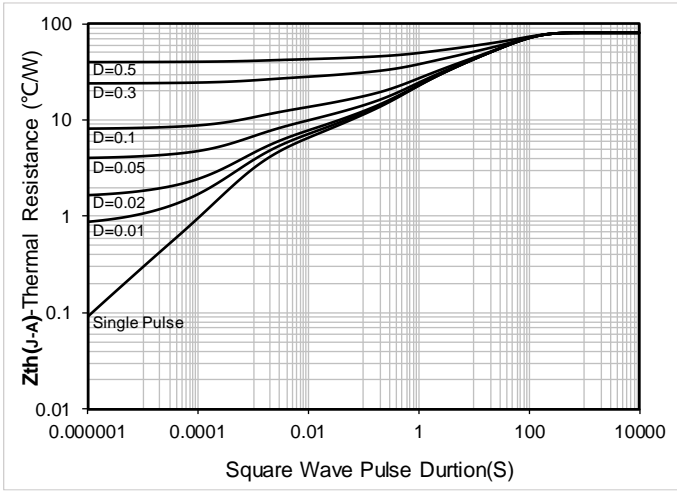


Figure 13. Maximum Transient Thermal Impedance

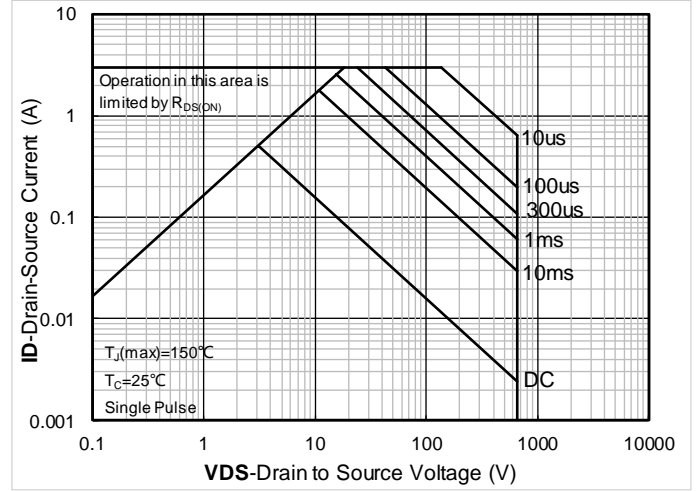


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

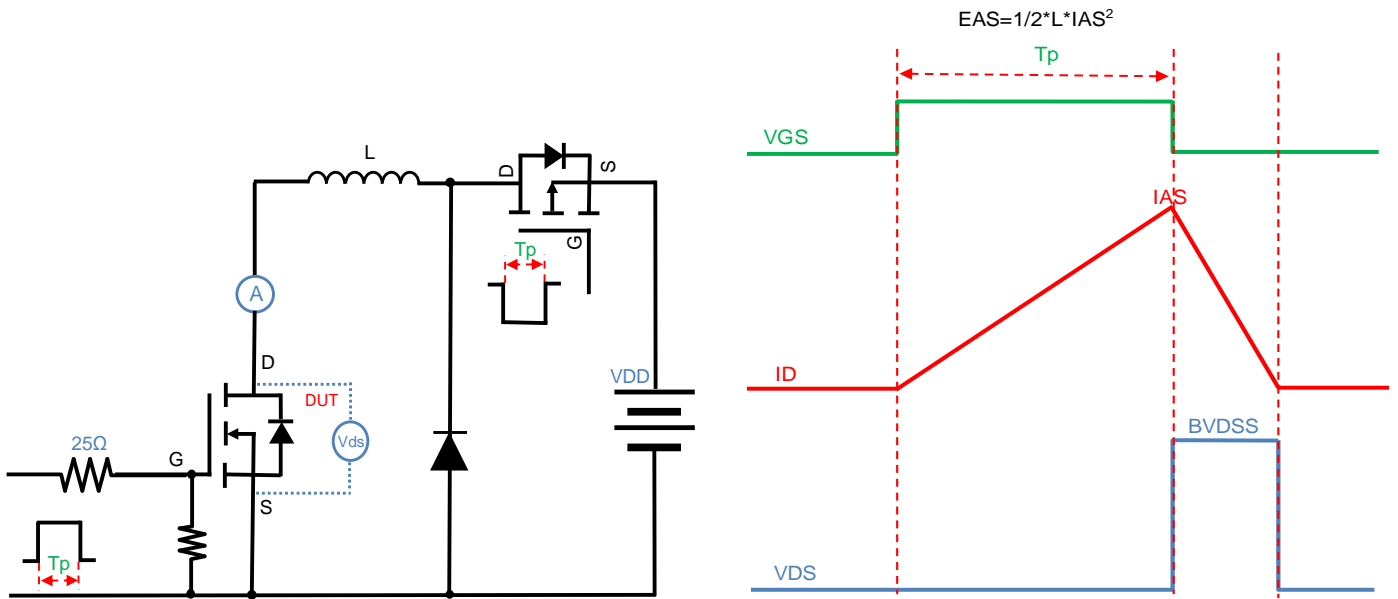


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

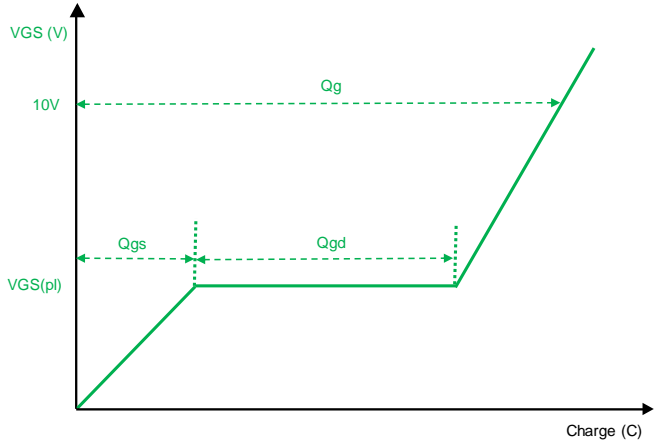
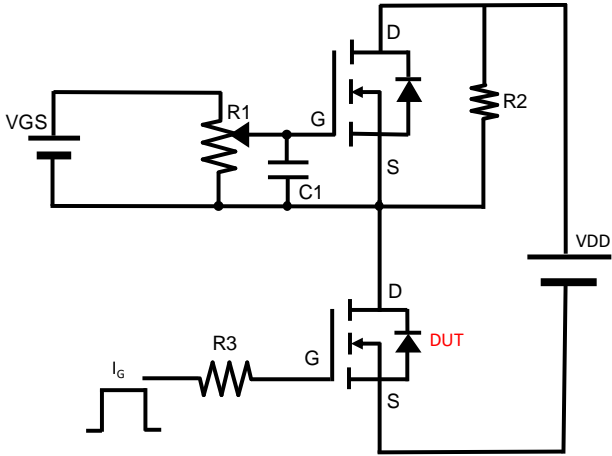


Figure B. Gate Charge Test Circuit & Waveform

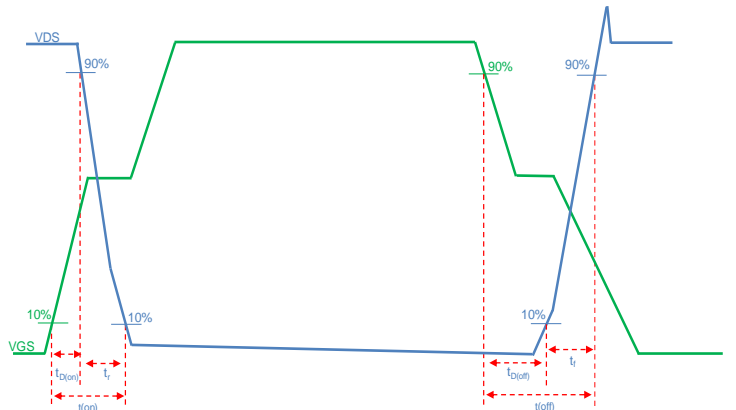
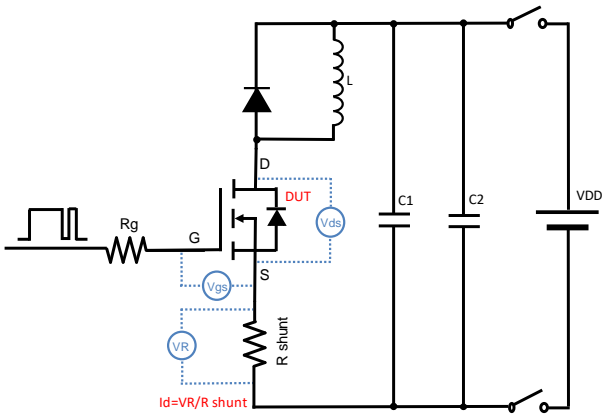


Figure C. Resistive Switching Test Circuit & Waveform

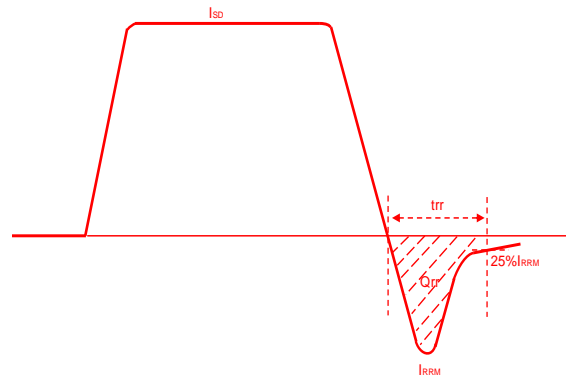
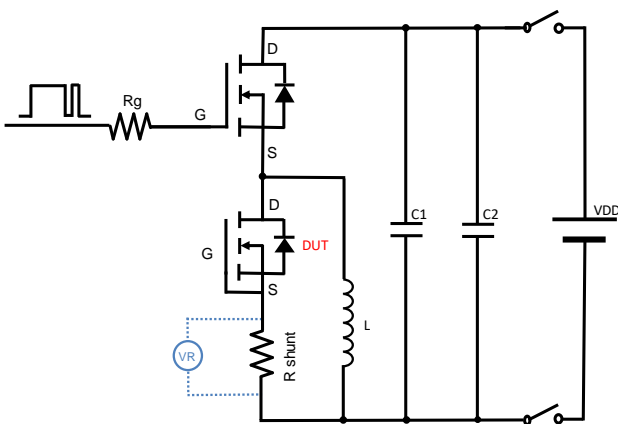
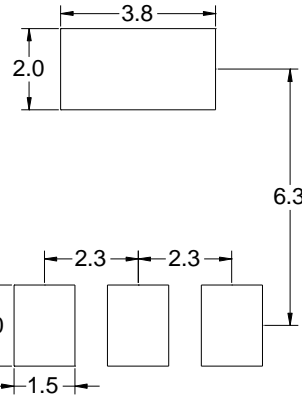
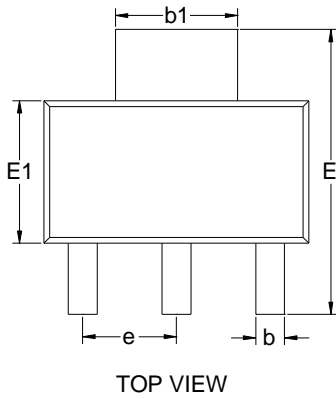
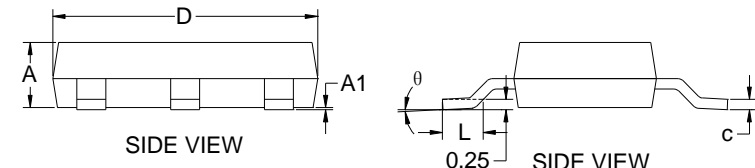


Figure D. Diode Recovery Test Circuit & Waveform



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■ SOT-223 Package information



SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
DIM	INCHES		MM	
	MIN	MAX	MIN	MAX
A	0.0591	0.0670	1.5000	1.7000
A1	0.0008	0.0039	0.0200	0.1000
b	0.0259	0.0330	0.6600	0.8400
b1	0.1140	0.1220	2.9000	3.1000
c	0.0090	0.0138	0.2300	0.3500
D	0.2480	0.2640	6.3000	6.7000
E	0.2637	0.2874	6.7000	7.3000
E1	0.1290	0.1460	3.3000	3.7000
e	0.0866	0.0945	2.2000	2.4000
L	0.0295	0.0492	0.7500	1.2500
θ	0°	10°	0°	10°



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